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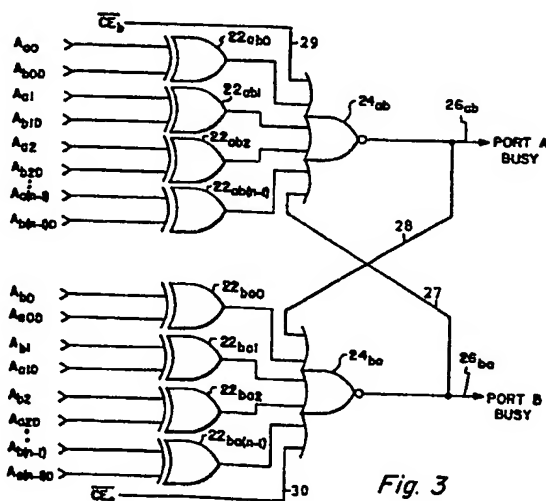
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64 Address contention arbitrator for multi-port memories.

57 For detecting and resolving address contention between ports of a multi-port memory address signals ($A_{a0} - A_{a(n-1)}$) arriving at a first port (A) are compared with delayed address signals ($A_{b00} - A_{b(n-1)0}$) from a second port (B). If a match occurs, the second port (B) is given priority. Similarly address signals ($A_{b0} - A_{b(n-1)}$) arriving at the second port (B) are compared with delayed address signals ($A_{a00} - A_{a(n-1)0}$) arriving at the first port (A). If a match occurs in the comparison, the first port (A) is given priority.



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ADDRESS CONTENTION ARBITRATOR FOR
MULTI-PORT MEMORIES

5 The present invention relates to multi-port
electronic memories and more particularly to systems
for detecting and arbitrating contention between the
ports thereof.

10 A block of electronic memory is typically
organized into individual memory locations each of
which contain one or more binary digits (bits). Each
such location has associated therewith an address. In
order to read information from a particular memory
15 location or to write information into that memory
location, that location address is transmitted to the
memory on an address bus. The address signal is
typically provided as an n bit signal where n is a
positive integer.

20 Often a particular application will require
that more than one processor, or other type of
circuitry, be allowed to access memory locations in
the same block of memory. Various approaches have

been used in order to allow this. Under one approach
circuitry is provided to give each circuit requiring
access to the block of memory exclusive access at
certain times. While this will work in some
5 circumstances under other circumstances a preferable
arrangement would be to allow all circuits requiring
such access to have it simultaneously. Memory
circuits which allow a plurality of external circuits
access to memory locations within the same block of
10 memory at the same time are called dual or multi-port
memories. Such memories will have a plurality of
address inputs and a plurality of data input output
(I/O) ports. One data I/O port is associated with
each address input. If a read operation is to be
15 performed, circuitry associated with the memory will
provide the value stored in the memory at the location
specified on the address bus to the I/O port
associated with that address bus. Similarly, if a
write operation is to be performed the value arriving
20 at an I/O port is stored in the memory at the location
specified on the associated address bus.

Such an arrangement will work under most
circumstances. However, if two circuits both having
access to the memory attempt to access the same memory
25 location within that memory at the same time, problems
may arise. The situation may be particularly acute if

one of the circuits attempts to write information into a memory location while the other circuit is either reading from or writing to that same location. In order to prevent problems from arising under those
5 circumstances circuitry must be provided to determine which circuitry attempted to access the memory location first and to provide a busy signal to the other circuit. This busy signal prevents that circuit from accessing the memory until the first circuit has
10 completed its process. This problem is solved by the invention as characterized in claim 1.

The present invention provides a system for detecting address contention and resolving such
15 contention in a multi-port memory. In an embodiment having two ports, designated port A and port B, the system works by comparing the address signals arriving at port A with a delayed version of the address signals which arrived at port B. If, when the address
20 signals first arrive at port A, a match is found, address contention exists. Furthermore, since the port B address signals used in the comparison were delayed, clearly the port B address signals had to be there first in order for the match to occur.
25 Therefore, a busy signal is generated for port A until

port B completes its access of the memory location. Similar circuitry is provided for comparing current address signals at port B with delayed address signals from port A. This circuit in turn generates busy signals, when required, for port B. The system may be expanded for use with more than two ports by providing additional delay and comparison circuits. Further details and improvements are described in the subclaims. The invention is explained in detail by reference to an embodiment shown in the drawings; wherein

Figure 1 shows the arrangement for conditioning address signals for comparison;

Figure 2 shows an example of a delay circuit which could be used with the invention; and

Figure 3 shows the address comparison and busy signal generator of the invention.

The present invention will be described for a two port memory. Those skilled in the art will readily see that it is not limited to such use, however, and could be used in systems having more than two ports. Furthermore, each address will be assumed to have n bits where n is a positive integer. Although only four address lines are shown for each address port, typically n would be greater than four.

The address signals arriving at the port A address input will be designated A_{a0} , A_{a1} , ... $A_{a(n-1)}$. The delayed version of those signals will be designated A_{a0D} , A_{a1D} , ..., $A_{a(n-1)D}$. Similar designations are
5 used for the address signals arriving at the port B address input.

In the system of Figure 1 the signal A_{a0} arrives and is applied to signal line 10_{a0} . Signal line 10_{a0} is electrically connected to time delay
10 generator 12_{a0} and to output region 14_{a0} . Time delay generator 12_{a0} is electrically connected to output region 16_{a0} . Therefore, the original address signal A_{a0} is available at output region 14_{a0} and the delayed address signal A_{a0D} is available at output region
15 16_{a0} . Similarly, delayed versions of the remaining address signals arriving at the port A address input are also produced and provided at appropriate output regions. Likewise, the remaining original address signals arriving at the port A address input
20 are provided at their appropriate output regions. As also shown in Figure 1 similar current and delayed address signals are provided for those address signals arriving at the port B address input.

Figure 2 illustrates an example of an
25 electronic system which could be used as an electronic delay such as delay generator 12_{a0} of Figure 1. In

this embodiment the delay is simply two electronic
inverters 18_{a0} and 20_{a0}. The gate delay of the
inverters is sufficient to be the delay for the
invention. The use of two inverters to provide the
delay is preferred in most systems because inverters
may be easily provided. The invention is not limited
to the use of a pair of inverters, however, and other
methods of providing the delay may be used.

Turning now to Figure 3 the system for
determining whether address contention exists, and
resolving it if it does, is shown. In Figure 3 are
shown a series of EXCLUSIVE OR gates, 22_{ab0}, 22_{ab1},
22_{ab2}, 22_{ab(n-1)}, 22_{ba0}, 22_{ba1}, 22_{ba2}, and 22_{ba(n-1)}.
In Figure 3 the use of the subscript ab indicates that
the undelayed a signal is combined with the delayed b
signal in that EXCLUSIVE OR gate, and the use of the
subscript ba indicates the opposite. The number in
each subscript indicates the order number of the
address bit which is combined in that EXCLUSIVE OR
gate. Following this convention EXCLUSIVE OR gate
22_{ab0} combines the current signal A_{a0} and the delayed
signal A_{b0D}. If the signals A_{a0} and A_{b0D} are both
zero or both one the output of EXCLUSIVE OR gate 22_{ab0}
will be zero. If the signals A_{a0} and A_{b0D} differ from

one another, however, the output of EXCLUSIVE OR gate 22_{ab0} will be equal to one. Similarly, the other EXCLUSIVE OR gates produce output signals based on the input signals received.

5 The outputs from each of EXCLUSIVE OR gates 22_{ab0} through 22_{ab(n-1)} serve as input signals to NOR gate 24_{ab}. Similarly, the output signals from EXCLUSIVE OR gates 22_{ba0} through 22_{ba(n-1)} serve as input signals to NOR gate 24_{ba}. Furthermore, the
10 output signal from NOR gate 24_{ba} serves via line 27 as an input signal for NOR gate 24_{ab} and the output signal from NOR gate 24_{ab} serves via line 28 as an input signal to NOR gate 24_{ba}. Each of NOR gates 24_{ab} and 24_{ba} have provided thereto as additional input signals CE_b and CE_a,
15 respectively. Not all memory systems use the CE_a and CE_b signals, and they are not required by the invention. Therefore, the invention will first be described without these signals.

 According to the standard operation of a NOR
20 gate if any input signal to either of NOR gates 24_{ab} or 24_{ba} is one the output of that NOR gate will be zero. If all of the inputs to either of NOR gates 24_{ab} or 24_{ba} are equal to zero the output of that NOR gate will be equal to one.

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The operation of the system of Figure 3 will now be explained, assuming that initially no address contention exists. When that is the case, at least one of the bits presented at port A must differ from the corresponding bit presented at port B. Therefore, at least one of EXCLUSIVE OR gates 22_{ab0} through 22_{ab(n-1)} must receive differing input signals, and thus provide an output signal equal to one.

Therefore, at least one of the input signals to NOR gate 24_{ab} must be equal to one causing NOR gate 24_{ab} to have an output signal equal to zero. Similarly, NOR gate 24_{ba} must receive at least one input signal equal to one and so will produce an output signal equal to zero.

If a memory operation is initiated by a call through port B, a memory location address will be transmitted to the port B address input. That address is applied to input lines A_{b0} through A_{b(n-1)}. A short time later that same address will be applied, in delayed form, to lines A_{b0D} through A_{b(n-1)D}. If a memory operation is then initiated through port A, the address called will be applied to input lines A_{a0} through A_{a(n-1)}. If the same memory location has been addressed through both ports A and B the input signals to each of EXCLUSIVE OR gates 22_{ab0} through 22_{ab(n-1)}

will be either two ones or two zeros. Therefore, each of EXCLUSIVE OR gates 22_{ab0} through $22_{ab(n-1)}$ will produce an output signal equal to zero. As explained previously, NOR gate 24_{ba} is producing an output equal to zero also. Therefore, all input signals to NOR gate 24_{ab} are equal to zero and thus that NOR gate produces an output signal equal to one. This signal is used as a busy signal to prevent port A from having access to the requested memory location until port B has completed its access. Furthermore, the fact that the output signal from NOR gate 24_{ab} is used as an input signal to NOR gate 24_{ba} insures that NOR gate 24_{ba} will continue to receive at least one input signal equal to one even after the delayed address sent to port A arrives at the input lines to EXCLUSIVE OR gates 22_{ba0} through $22_{ba(n-1)}$. In that way, port B will not receive a busy signal.

The above description explains how the present invention detects memory contention and resolves it in favor of port B, if port B were the first port to be addressed. Similarly, contention would be detected and resolved in favor of port A if port A were the first port to be addressed. If the two ports are simultaneously addressed both will attempt to produce a busy signal and allow access to the other port. In theory this could cause the system

to lock out all further attempted memory accesses. In reality, however, even if NOR gates 24_{ab} and 24_{ba} were designed to be identical, processing variations would be expected to cause NOR gates 24_{ab} and 24_{ba} to differ enough so as to prevent such lock out. Specifically, one of those gates will typically have greater capacitance than the other. The gate with higher capacitance will be able to force the other to a zero output value. This design could be left to chance so that either port A or port B would have precedence in a simultaneous addressing situation, or one gate or the other could be intentionally designed to have greater capacitance, insuring that all memories produced would have a preselected one of ports A and B having precedence.

The discussion above has not dealt with the signals CE_a and CE_b . These are chip enable signals which are used in some, but not all, memory systems. Signal CE_a is equal to zero when a memory operation is occurring through port A and equal to one if no such operation is occurring. Similarly, CE_b is equal to zero if a memory operation is occurring through port B and is equal to one if no such operation is occurring. If the memory system in which the invention is to be used utilizes such chip enable signals, signal $\overline{CE_b}$ should be connected via line 29 to NOR

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gate 24_{ab} and signal \overline{CE}_a should be connected via line 30 to NOR gate 24_{ba} as is shown in Figure 3. When this is done a port is not considered to have begun addressing the memory until the proper address location has been transmitted to that port and the
5 associated chip enable signal has gone to a value of zero.

As explained previously, this discussion has described a system for detecting and resolving memory contention in a dual port ram. Those skilled in the
10 art will readily see that the same system could be used with more than two ports. If a third port, port C, were added a similar circuit would be provided to resolve contention between A and C. A third similar circuit would be required to resolve contention
15 between ports B and C. Thus any number of ports could be accommodated under the present invention, simply by providing circuits to resolve contention between each pair of ports.

Claims:

1. Address contention detection and arbitration system for a memory having at least first (A) and second (B) ports, said first and second ports being adapted to receive first and second address signals,
 5 respectively, characterized by
 - a) first ($12_{a0} - 12_{a(n-1)}$) and second ($12_{b0} - 12_{b(n-1)}$) delay means for producing first and second delayed address signals from said first ($A_{a0} - A_{a(n-1)}$) and second ($A_{b0} - A_{b(n-1)}$) address signals,
 10 respectively;
 - b) first comparison means ($22_{ab0} - 22_{ab(n-1)}$) for comparing said first address signal with said second delayed address signal and generating a busy signal for said first port if said first address signal and said second
 15 delayed address signal are identical;
 - c) second comparison means ($22_{ba0} - 22_{ba(n-1)}$) for comparing said second address signal with said first delayed address signal and generating a busy signal for said second port if said second address signal and said
 20 first delayed address signal are identical;
 - d) first suppression means (27) to prevent said first comparison means from generating a busy signal for said first port (A) when said second comparison means is generating a busy signal for said second port (B); and
 25 e) second suppression means (28) to prevent said second comparison means from generating a busy signal for said second port (B) when said first comparison means is generating a busy signal for said first port (A).
- 30 2. The system of claim 1, characterized in that said first and second address signals are n bit binary digital signals, where n is a positive integer, and each of said comparison means (22) includes n EXCLUSIVE OR gate.
- 35 3. The system of claim 2, characterized in

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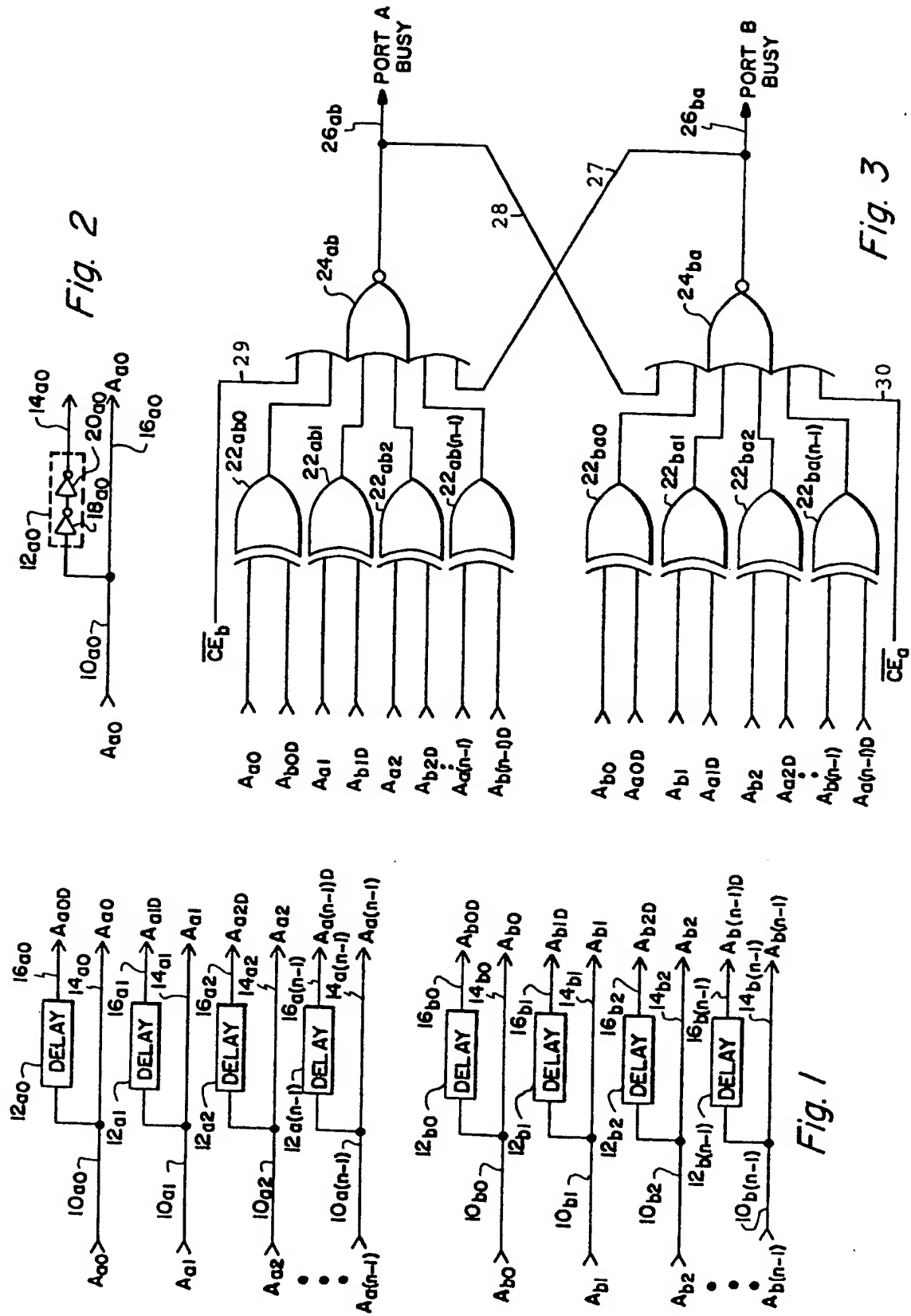
- 5 t h a t each of said EXCLUSIVE OR logic gates has first and second inputs and an output, said EXCLUSIVE OR gate of said first comparison means ($22_{ab0} - 22_{ab(n-1)}$) being adapted to accept a signal representative of one bit of said n bits of said first address signal on said first input and a corresponding bit of said n bits of said second delayed address signal on said second input, and each of said EXCLUSIVE OR gates of said second comparison means being adapted to accept one bit of said n bits of said second address signal on said first input and one bit of said n bits of said first delayed address signal on said second input.
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- 15 4. The system of claim 3, c h a r a c t e r i z e d i n t h a t each of said first and second comparison means includes a combining logic gate ($24_{ab}; 24_{ba}$).
- 20 5. The system of claim 4, c h a r a c t e r i z e d i n t h a t said combining logic gates ($24_{ab}, 24_{ba}$) are NOR logic gate means having a plurality of inputs, each of said outputs of said EXCLUSIVE OR logic gates ($22_{ab0} - 22_{ab(n-1)}$) of said first comparison means (22_{ab}) being electrically connected to one of said inputs of said first comparison NOR gates (24_{ab}), and each of said outputs of said EXCLUSIVE OR gates ($22_{ba0} - 22_{ba(n-1)}$) of said second comparison means (22_{ba}) being electrically connected to one of said inputs of said second comparison NOR gates (24_{ba}).
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- 30 6. The system of claim 5, c h a r a c t e r i z e d i n t h a t said first suppression means comprises an electrically conducting means (27) electrically connecting said second comparison NOR gate (24_{ba}) output (26_{ba}) with one of said inputs of said first comparison NOR gates (24_{ab}) and said second suppression means includes an electrically conducting means (28) electrically connecting said first comparison NOR gate (24_{ab}) output (26_{ab}) with one of said inputs of said second comparison NOR gate (24_{ba}).
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7. An address contention detection and arbitration system for a memory having first and second ports, said first and second ports being adapted to receive first and second address signals, respectively, each of said address signals being an n bit binary digital signal where n is a positive integer, characterized by :
- 5 A) first ($12_{ab0} - 12_{ab(n-1)}$) and second ($12_{ba0} - 12_{ba(n-1)}$) means for producing first and second delayed address signal from said first and second address signals, respectively;
- 10 B) first plurality of EXCLUSIVE OR logic gates ($22_{ab0} - 22_{ab(n-1)}$), each of said EXCLUSIVE OR logic gates of said first plurality thereof having first and second input means and output means, each of said first input means of said EXCLUSIVE OR logic gates of said first plurality thereof being adapted to accept as an input signal one bit of said n bits of said first address signal and each of said second input means of said EXCLUSIVE OR logic gates of said first plurality thereof being adapted to accept as an input signal a corresponding bit of said n bits of said second delayed address signal;
- 15 C) second plurality of EXCLUSIVE OR logic gates ($22_{ba0} - 22_{ba(n-1)}$), each of said EXCLUSIVE OR logic gates of said second plurality thereof having first and second input means and output means, each of said first input means of said EXCLUSIVE OR logic gates of said second plurality thereof being adapted to accept as an input signal one bit of said n bits of said second address signal and each of said second input means of said EXCLUSIVE OR logic gates of said second plurality thereof being adapted to accept as an input signal a corresponding bit of said n bits of said first delayed address signal;
- 20 D) first NOR logic gates (24_{ab}) having a plurality of input means and an output means, each of said output means of said EXCLUSIVE OR logic gates of said first plurality thereof being electrically connected to one
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- of said input means of said first NOR logic gates;
- E) second NOR (24_{ba}) logic gates having a plurality of input means and an output means, each of said output means of said EXCLUSIVE OR gates of said second plurality thereof being electrically connected to one of of said input means of said second NOR logic gates;
- 5 F) first electrical conducting means (27) electrically connecting said second NOR logic gate (24_{ba}) output (26_{ba}) with one of said first NOR logic gates input means; and
- 10 G) second electrical conducting means (28) electrically connecting said first NOR logic gate (24_{ab}) output (26_{ab}) with one of said second NOR logic gate means input means.
- 15 8. The system of one of the preceding claims, characterized by
- H) said first (A) and second (B) ports having associated therewith respectively, first (\overline{CE}_a) and second (\overline{CE}_b) chip enable signal input means,
- 20 I) first electrical connecting means (29) provided between said second chip enable signal input (\overline{CE}_b) and one of said first NOR gate (24_{ab}) inputs; and
- 25 J) second electrical connecting means (30) provided between said first chip enable signal input (\overline{CE}_a) and one of said inputs of said second NOR gate (24_{ba}).
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EUROPEAN SEARCH REPORT

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EP 86 10 1935

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
X	EP-A-0 106 557 (WESTERN ELECTRIC CO.) * Figures 1,2; page 9, lines 21-37 *	1	G 06 F 13/18
A	--- ELECTRONICS INTERNATIONAL, vol. 55, no. 20, October 1982, pages 47-48, New York, US; W.R. IVERSEN: "Dual-port RAM transfers data more efficiently" * Page 47, left-hand column, lines 16-23 * -----	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl. 4)
			G 06 F 13/18 G 06 F 13/16
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 02-06-1986	Examiner CRECHET P.G.M.
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	